CLAIMS

What is claimed is:

1. An apparatus comprising:

an oscillator; and

a delay unit to provide a delay in response to an output of the oscillator, and to provide an output to be used as a power-on reset signal.

2. The apparatus according to claim 1, wherein the delay unit is logic that provides a delay in response to an input signal.

3. The apparatus according to claim 1, wherein the delay unit is a counter.

4. The apparatus according to claim 3, wherein the counter is at least one of a binary counter, a decimal counter and a shift register counter.

5. The apparatus according to claim 1, wherein the oscillator is at least one of a ring oscillator, an LC oscillator and an RTC oscillator.

6. The apparatus according to claim 1, wherein elements of the delay unit and the oscillator are chosen to have similar power-on behavior to an electronic device in which the apparatus is included.

7. The apparatus according to claim 1, wherein elements of the delay unit and the oscillator are chosen to have similar power-on behavior elements in a library used to design an electronic device in which the apparatus is included.

8. The apparatus according to claim 1, wherein elements of the delay unit and the oscillator are chosen from elements in a library used to design an electronic device in which the apparatus is included.

9. The apparatus according to claim 1, wherein the oscillator includes at least one inverter.

10. The apparatus according to claim 3, wherein the counter includes at least one latch.

11. The apparatus according to claim 10, wherein at least one latch in the counter favors a known state.

12. The apparatus according to claim 10, wherein each latch in the counter favors a known state.

13. The apparatus according to claim 10, wherein the counter includes at least two latches, and at least a most significant bit latch of the latches in the counter favors a known state.

14. The apparatus according to claim 1, wherein the power-on reset signal is provided to enable the oscillator.

15. The apparatus according to claim 14, further comprising a NAND gate having an input coupled to the power-on reset signal and an output coupled to an input of the oscillator, the NAND gate to enable the oscillator.

16. The apparatus according to claim 1, further comprising a buffer at an output of the delay unit to provide the power-on reset signal.

17. The apparatus according to claim 16, wherein the buffer is an inverter.

18. The apparatus according to claim 16, wherein the buffer is coupled to an output of the delay unit.

19. The apparatus according to claim 16, wherein the buffer is included in the delay unit.

20. The apparatus according to claim 1, wherein the apparatus is included in an electronic device and the power-on reset signal is provided within the electronic device.

21. The apparatus according to claim 20, wherein the electronic device is at least one of an integrated circuit, a chip, a chip set, a digital electronic device, a micro-

controller, a microprocessor, a controller, a processor, a small form factor device, a cell phone, a cell phone chip, a cell phone chip set, a next generation cell phone, a next generation cell phone chip, a next generation cell phone chip set, an electronic circuit, an embedded micro-controller, a telecommunications device, a speaker phone, and an electronic device with state retention.

22. The apparatus according to claim 1, wherein the apparatus is included in an electronic device and the power-on reset signal is provided externally from the electronic device.

23. A system comprising:

an electronic device, including:

an oscillator; and

a delay unit to provide a delay in response to an output of the oscillator, and to provide an output to be used as a power-on reset signal.

24. The system according to claim 23, wherein the delay unit is logic that provides a delay in response to an input signal.

25. The system according to claim 23, wherein the delay unit is a counter.

26. The system according to claim 25, wherein the counter is at least one of a binary counter, a decimal counter and a shift register counter.

27. The system according to claim 23, wherein the oscillator is at least one of a ring oscillator, an LC oscillator and an RTC oscillator.

28. The system according to claim 23, wherein elements of the delay unit and the oscillator are chosen to have similar power-on behavior to the electronic device.

29. The system according to claim 23, wherein elements of the delay unit and the oscillator are chosen to have similar power-on behavior elements in a library used to design the electronic device.

30. The system according to claim 23, wherein elements of the delay unit and the oscillator are chosen from elements in a library used to design the electronic device.

31. The system according to claim 23, wherein the oscillator includes at least one inverter.

32. The system according to claim 25, wherein the counter includes at least one latch.

33. The system according to claim 32, wherein at least one latch in the counter favors a known state.

34. The system according to claim 32, wherein each latch in the counter favors a known state.

35. The system according to claim 32, wherein the counter includes at least two latches, and at least a most significant bit latch of the latches in the counter favors a known state.

36. The system according to claim 23, wherein the power-on reset signal is provided to enable the oscillator.

37. The system according to claim 36, further comprising a NAND gate having an input coupled to the power-on reset signal and an output coupled to an input of the oscillator, the NAND gate to enable the oscillator.

38. The system according to claim 23, further comprising a buffer at an output of the delay unit to provide the power-on reset signal.

39. The system according to claim 38, wherein the buffer is an inverter.

40. The apparatus according to claim 38, wherein the buffer is coupled to an output of the delay unit.

41. The apparatus according to claim 38, wherein the buffer is included in the delay unit.

42. The system according to claim 23, wherein the power-on reset signal is provided within the electronic device.

43. The system according to claim 23, wherein the electronic device is at least one of an integrated circuit, a chip, a chip set, a digital electronic device, a micro-controller, a microprocessor, a controller, a processor, a small form factor device, a cell phone, a cell phone chip, a cell phone chip set, a next generation cell phone, a next generation cell phone chip, a next generation cell phone chip set, an electronic circuit, an embedded micro-controller, a telecommunications device, a speaker phone, and an electronic device with state retention.

44. The system according to claim 23, wherein the power-on reset signal is provided externally from the electronic device.

45. A method comprising:

oscillating; and

delaying an output of the oscillating to provide a power-on reset signal.

46. The method according to claim 45, wherein the delaying of the output of the oscillating is provided by counting.

47. The method according to claim 45, further comprising providing the power-on reset signal to enable the oscillating.

48. The method according to claim 45, wherein the power-on reset signal is provided within an electronic device.

49. The method according to claim 48, wherein the electronic device is at least one of an integrated circuit, a chip, a chip set, a digital electronic device, a micro-controller, a microprocessor, a controller, a processor, a small form factor device, a cell phone, a cell phone chip, a cell phone chip set, a next generation cell phone, a next generation cell phone chip, a next generation cell phone chip set, an electronic circuit, an embedded micro-controller, a telecommunications device, a speaker phone, and an electronic device with state retention.

50. The method according to claim 45, wherein the power-on reset signal is provided externally from an electronic device.

51. The method according to claim 46, wherein the counting counts a designated number of cycles, wherein the power-on reset signal is asserted when the counting

3 begins counting the designated number of cycles and is de-asserted when the counting

4 finishes counting the designated number of cycles.